6C-QSFP+-LR4

6COM, QSFP+,40Gb/s , 1271~1331nm,SMF, 10KM, DDM,LC connector, 0°C to 70°C

PRODUCT FEATURES

◆ 4 CWDM lanes Mux/Demux design

◆ Up to 11.1Gbps Data rate per wavelength

◆ Up to 10km transmission on SMF

◆ Electrically hot-pluggable

◆ Digital Diagnostics Monitoring Interface

◆ Compliant with QSFP+ MSA with LC connector

◆ Case operating temperature range:0°C to 70°C

◆ Power dissipation < 2.5 W

APPLICATIONS

◆ 40G Ethernet

◆ Data Center and LAN

STANDARD

◆ Compliant to IEEE 802.3ba

◆ Compliant to SFF-8436

◆ RoHS Compliant.

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General Description

6C-QSFP+-LR4 is designed to operate over single-mode fiber system using 4X10 CWDM channel in 1310 band and links up to 10km. The module converts 4 inputs channel of 10Gb/s electrical data to 4 CWDMoptical signals, and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, onthe receiver side, the module optically de-multiplexes a 40Gb/s input into 4 CWDM channels signals, andconverts them to 4 channel output electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm. It contains a duplex LC connector for the optical interface and a 38-pin connector for the electrical interface.Single-mode fiber (SMF) is applied in this module. This product converts the 4-channel 10Gb/s electricalinput data into CWDM optical signals (light), by a 4-wavelength Distributed Feedback Laser (DFB) array.The 4 wavelengths are multiplexed into a single 40Gb/s data, propagating out of the transmitter modulevia the SMF. The receiver module accepts the 40Gb/s optical signals input, and de-multiplexes it into 4CWDM 10Gb/s channels. Each wavelength light is collected by a discrete photo diode, and thenoutputted as electric data after amplified by a TIA.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA) and compliant to 40G QSFP+ LR4 of IEEE 802.3ba.

1. Absolute Maximum Ratings

Parameter	Symb	Min.	Typ	Max.	Unit	Note
Storage Temperature	Ts	-40	-	85	ºC	
Relative Humidity	RH	5	-	95	%	
Power Supply Voltage	VCC	-0.3	-	4	V	
Signal Input Voltage		Vcc-	-	Vcc+0.	V	

2. Recommended Operating Conditions

Parameter	Symb	Min	Typ.	Max.	Unit	Note
Case Operating Temperature	Tcas	0	-	70	ºC	Without air
Power Supply Voltage	VCC	3.1	3.3	3.47	V	
Power Supply Current	ICC	-		760	mA	
Data Rate	BR		10.31		Gbp	Each
Transmission Distance	TD		-	10	km	
Coupled fiber	Single mode fiber					9/125um

3. Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Transmitter						
	λ0	1264.5	1271	1277.5	nm	
	λ1	1284.5	1291	1297.5	nm	

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Wavelength Assignment	λ2	1304.5	1311	1317.5	nm	
	λ3	1324.5	1331	1337.5	nm	
Total Output. Power	P_{OUT}			8.3	dBm	
Average Launch Power Per lane		-7		2.3	dBm	
Spectral Width (-20dB)	σ			1	nm	
SMSR		30			dB	
Optical Extinction Ratio	ER	3.5			dB	
Average launch Power off per lane	Poff			-30	dBm	
RIN	RIN			-128	dB/Hz	
Output Eye Mask	Compliant with IEEE 802.3ba					
Receiver						
Rx Sensitivity per lane（OMA）	R_{SENS}			-13.7	dBm	1
Input Saturation Power (Overload)	Psat	2.3			dBm	
Receiver Reflectance	Rr			-26	dB	

Notes:
1. Measured with a PRBS $2^{31}-1$ test pattern, @10.325Gb/s, BER<10^{-12} .

4. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Supply Voltage	Vcc	3.13	3.3	3.47	V	
Supply Current	Icc			760	mA	
Transmitter						
Input differential impedance	Rin		100		Ω	1
Differential data input swing	Vin,pp	180		1000	mV	
Transmit Disable Voltage	VD	Vcc–1.3		Vcc	V	
Transmit Enable Voltage	VEN	Vee		Vee+ 0.8	V	2
Transmit Disable Assert Time				10	us	
Receiver						
Differential data output swing	Vout,pp	300		850	mV	3
Data output rise time	tr	28			ps	4
Data output fall time	tf	28			ps	4
LOS Fault	VLOS fault	Vcc–1.3		VccHOST	V	5
LOS Normal	VLOS	Vee		Vee+0.8	V	5

Notes:

1. Connected directly to TX data input pins. AC coupled thereafter.

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2. Or open circuit.

3. Into 100 ohms differential termination.

4. 20 -80 %.

5. Loss Of Signal is LVTTL. Logic 0 indicates normal operation; logic 1 indicates no signal   detected.

5. Pin Assignment
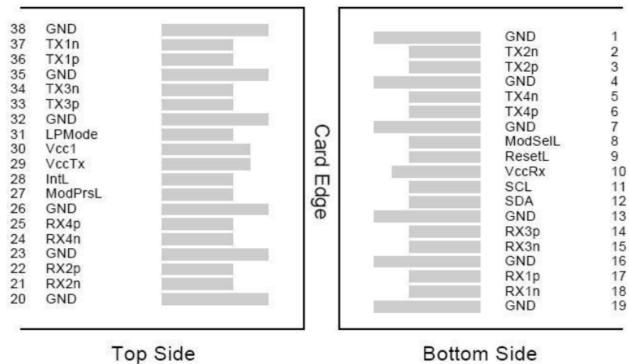


```
Top Side                          Bottom Side
38  GND                                GND   1
37  TX1n                              TX2n   2
36  TX1p                              TX2p   3
35  GND                               GND   4
34  TX3n                              TX4n   5
33  TX3p                              TX4p   6
32  GND               Card Edge       GND   7
31  LPMode                         ModSelL   8
30  Vcc1                            ResetL   9
29  VccTx                           VccRx   10
28  IntL                              SCL   11
27  ModPrsL                           SDA   12
26  GND                               GND   13
25  RX4p                             RX3p   14
24  RX4n                             RX3n   15
23  GND                               GND   16
22  RX2p                             RX1p   17
21  RX2n                             RX1n   18
20  GND                               GND   19
```

Figure 1---Pin out of Connector Block on Host Board

Pin	Symbol	Name/Description	NOT
1	GND	Transmitter Ground (Common with Receiver Ground)	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Transmitter Ground (Common with Receiver Ground)	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Transmitter Ground (Common with Receiver Ground)	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Transmitter Ground (Common with Receiver Ground)	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Transmitter Ground (Common with Receiver Ground)	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Transmitter Ground (Common with Receiver Ground)	1

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20	GND	Transmitter Ground (Common with Receiver Ground)	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Transmitter Ground (Common with Receiver Ground)	1
24	Rx4n	Receiver Inverted Data Output	1
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Transmitter Ground (Common with Receiver Ground)	1
27	ModPrsl	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	LPMode	Low Power Mode	
32	GND	Transmitter Ground (Common with Receiver Ground)	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Transmitter Ground (Common with Receiver Ground)	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Transmitter Ground (Common with Receiver Ground)	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP+ modules. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted.Connect these directly to the host board signal common ground plane.

2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Txmay be internally connected within the QSFP+ transceiver module in any combination. The connectorpins are each rated for a maximum current of 500mA.

6. Digital Diagnostic Functions

6C-QSFP+-LR4 support the 2-wire serial communication protocol as defined in the QSFP+ MSA.which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller inside the transceiver, which is accessed through the 2-wire serial interface. Whenthe serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positiveedge clocks data into the QSFP+ transceiver into those segments of its memory map that are notwrite-protected. The negative edge clocks data from the QSFP+ transceiver. The serial data signal (SDApin) is bi-directional for serial data transfer. The host uses SDA

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in conjunction with SCL to mark the startand end of serial protocol activation. The memories are organized as a series of 8-bit data words that canbe addressed individually or sequentially. The 2-wire serial interface provides sequential or randomaccess to the 8 bit parameters, addressed from 00h to the maximum address of the memory.

This clause defines the Memory Map for QSFP+ transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP+ devices. The memory map hasbeen changed in order to accommodate 4 optical channels and limit the required memory space. Thestructure of the memory is shown in Figure 2 -QSFP+ Memory Map. The memory space is arranged intoa lower, single page, address space of 128 bytes and multiple upper address space pages. This structurepermits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time criticalentries, e.g. serial ID information and threshold settings, are available with the Page Select function. Thestructure also provides address expansion by adding additional upper pages as needed. For example, inFigure 2 upper pages 01 and 02 are optional. Upper page 01 allows implementation of ApplicationSelect Table, and upper page 02 provides user read/write space.　The lower page and upper pages 00 and 03 are always implemented. The interface address used is A0xh and is mainly used for time critical datalike interrupt handling in order to enable a "one-time-read" for all data related to an interrupt situation.After an Interrupt, IntL, has been asserted, the host can read out the flag field to determine the effectedchannel and type of flag.

For more detailed information including memory map definitions, please see the QSFP+ MSA
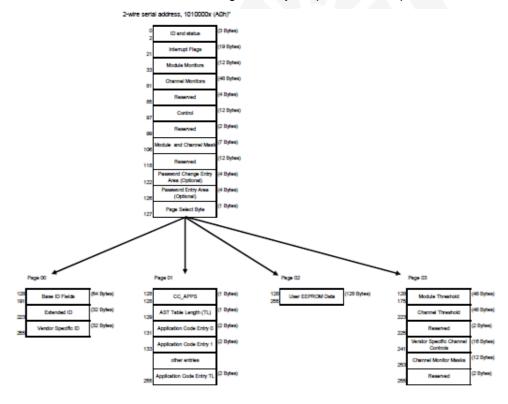

Figure 2 –QSFP+ Memory Map

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Specification.

Lower Memory Map

The lower 128 bytes of the 2-wire serial bus address space, see Table 1, is used to access a variety of measurements and diagnostic functions, a set of control functions, and a means to select which of thevarious upper memory map pages are accessed on subsequent reads. This portion of the address space isalways directly addressable and thus is chosen for monitoring and control functions that may need to berepeatedly accessed. The definition of identifier field is the same as page 00h Byte 128.

Table 1— Lower Memory Map

Byte Address	Description	Type
0	Identifier (1 Byte)	Read-Only
1-2	Status (2 Bytes)	Read-Only
3-21	Interrupt Flags (19 Bytes)	Read-Only
22-33	Module Monitors (12 Bytes)	Read-Only
34-81	Channel Monitors (48 Bytes)	Read-Only
82-85	Reserved (4 Bytes)	Read-Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Password Change Entry Area (optional) (4 Bytes)	Read/Write
123-126	Password Entry Area (optional) (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Status Indicator Bits

The Status Indicators are defined in Table 2.

Table 2 — Status Indicators

Byte	Bit	Name	Description
1	All	Reserved	
2	7	Reserved	
	6	Reserved	
	5	Reserved	
	4	Reserved	
	3	Reserved	
	2	Reserved	
	1	IntL	Digital state of the IntL interrupt output pin.
	0	Data_Not_Ready	Indicates transceiver has not yet achieved power up and monitor datais not ready. Bit remains high until data is ready to be read at which

Interrupt Flags

A portion of the memory map (Bytes 3 through 21), form a flag field. Within this field, the status of LOSand Tx Fault as well as alarms and warnings for the various monitored items is reported. For normal operation and default state, the bits in this field have the value of 0b. For the defined conditions of LOS,Tx Fault, module and channel alarms and warnings, the appropriate bit or bits are set, value = 1b. Onceasserted, the bits remained set (latched) until cleared by a read operation that includes the affected bit orreset by the ResetL pin. The Channel Status Interrupt Flags are defined in Table 3.

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Table 3 — Channel Status Interrupt Flags

Byte	Bit	Name	Description
3	7	L-Tx4 LOS	Latched TX LOS indicator, channel 4 (Not support)
	6	L-Tx3 LOS	Latched TX LOS indicator, channel 3 (Not support)
	5	L-Tx2 LOS	Latched TX LOS indicator, channel 2 (Not support)
	4	L-Tx1 LOS	Latched TX LOS indicator, channel 1 (Not support)
	3	L-Rx4 LOS	Latched RX LOS indicator, channel 4
	2	L-Rx3 LOS	Latched RX LOS indicator, channel 3
	1	L-Rx2 LOS	Latched RX LOS indicator, channel 2
	0	L-Rx1 LOS	Latched RX LOS indicator, channel 1
4	7-4	Reserved	
	3	L-Tx4 Fault	Latched TX fault indicator, channel 4
	2	L-Tx3 Fault	Latched TX fault indicator, channel 3
	1	L-Tx2 Fault	Latched TX fault indicator, channel 2
	0	L-Tx1 Fault	Latched TX fault indicator, channel 1
5	All	Reserved	

The Module Monitor Interrupt Flags are defined in Table 4.

Table 4 — Module Monitor Interrupt Flags

Byte	Bit	Name	Description
6	7	L-Temp High Alarm	Latched high temperature alarm
	6	L-Temp Low Alarm	Latched low temperature alarm
	5	L-Temp High Warning	Latched high temperature warning
	4	L-Temp Low Warning	Latched low temperature warning
	3-0	Reserved	
7	7	L-Vcc High Alarm	Latched high supply voltage alarm
	6	L-Vcc Low Alarm	Latched low supply voltage alarm
	5	L-Vcc High Warning	Latched high supply voltage warning
	4	L-Vcc Low Warning	Latched low supply voltage warning
	3-0	Reserved	
8	All	Reserved	

The Channel Monitor Interrupt Flags are defined in Table 5

Table 5 — Channel Monitor Interrupt Flags

Byte	Bit	Name	Description
9	7	L-Rx1 Power High Alarm	Latched high RX power alarm, channel 1
	6	L-Rx1 Power Low Alarm	Latched low RX power alarm, channel 1
	5	L-Rx1 Power High Warning	Latched high RX power warning, channel 1
	4	L-Rx1 Power Low Warning	Latched low RX power warning, channel 1
	3	L-Rx2 Power High Alarm	Latched high RX power alarm, channel 2
	2	L-Rx2 Power Low Alarm	Latched low RX power alarm, channel 2
	1	L-Rx2 Power High Warning	Latched high RX power warning, channel 2
	0	L-Rx2 Power Low Warning	Latched low RX power warning, channel 2
10	7	L-Rx3 Power High Alarm	Latched high RX power alarm, channel 3
	6	L-Rx3 Power Low Alarm	Latched low RX power alarm, channel 3
	5	L-Rx3 Power High Warning	Latched high RX power warning, channel 3
	4	L-Rx3 Power Low Warning	Latched low RX power warning, channel 3
	3	L-Rx4 Power High Alarm	Latched high RX power alarm, channel 4
	2	L-Rx4 Power Low Alarm	Latched low RX power alarm, channel 4
	1	L-Rx4 Power High Warning	Latched high RX power warning, channel 4
	0	L-Rx4 Power Low Warning	Latched low RX power warning, channel 4

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11	7	L-Tx1 Bias High Alarm	Latched high TX bias alarm, channel 1
	6	L-Tx1 Bias Low Alarm	Latched low TX bias alarm, channel 1
	5	L-Tx1 Bias High Warning	Latched high TX bias warning, channel 1
	4	L-Tx1 Bias Low Warning	Latched low TX bias warning, channel 1
	3	L-Tx2 Bias High Alarm	Latched high TX bias alarm, channel 2
	2	L-Tx2 Bias Low Alarm	Latched low TX bias alarm, channel 2
	1	L-Tx2 Bias High Warning	Latched high TX bias warning, channel 2
	0	L-Tx2 Bias Low Warning	Latched low TX bias warning, channel 2
12	7	L-Tx3 Bias High Alarm	Latched high TX bias alarm, channel 3
	6	L-Tx3 Bias Low Alarm	Latched low TX bias alarm, channel 3
	5	L-Tx3 Bias High Warning	Latched high TX bias warning, channel 3
	4	L-Tx3 Bias Low Warning	Latched low TX bias warning, channel 3
	3	L-Tx4 Bias High Alarm	Latched high TX bias alarm, channel 4
	2	L-Tx4 Bias Low Alarm	Latched low TX bias alarm, channel 4
	1	L-Tx4 Bias High Warning	Latched high TX bias warning, channel 4
	0	L-Tx4 Bias Low Warning	Latched low TX bias warning, channel 4
13	7	L-Tx1 Power High Alarm	Latched high TX Power alarm, channel 1
	6	L-Tx1 Power Low Alarm	Latched low TX Power alarm, channel 1
	5	L-Tx1 Power High Warning	Latched high TX Power warning, channel 1
	4	L-Tx1 Power Low Warning	Latched low TX Power warning, channel 1
	3	L-Tx2 Power High Alarm	Latched high TX Power alarm, channel 2
	2	L-Tx2 Power Low Alarm	Latched low TX Power alarm, channel 2
	1	L-Tx2 Power High Warning	Latched high TX Power warning, channel 2
	0	L-Tx2 Power Low Warning	Latched low TX Power warning, channel 2
14	7	L-Tx3 Power High Alarm	Latched high TX Power alarm, channel 3
	6	L-Tx3 Power Low Alarm	Latched low TX Power alarm, channel 3
	5	L-Tx31 Power High Warning	Latched high TX Power warning, channel 3
	4	L-Tx3 Power Low Warning	Latched low TX Power warning, channel 3
	3	L-Tx4 Power High Alarm	Latched high TX Power alarm, channel 4
	2	L-Tx4 Power Low Alarm	Latched low TX Power alarm, channel 4
	1	L-Tx4 Power High Warning	Latched high TX Power warning, channel 4
	0	L-Tx4 Power Low Warning	Latched low TX Power warning, channel 4
15-16	All	Reserved	Reserved channel monitor flags, set 4
17-18	All	Reserved	Reserved channel monitor flags, set 5
19-20	All	Reserved	Reserved channel monitor flags, set 6
21	All	Reserved	

Module Monitors

Real time monitoring for the QSFP+ module include transceiver temperature, transceiver supply voltage, and monitoring for each transmit and receive channel. Measured parameters are reported in 16-bit data fields, i.e., two concatenated bytes. These are shown in Table 6.

Table 6 — Module Monitoring Values

Byte	Bit	Name	Description
22	All	Temperature MSB	Internally measured module temperature
23	All	Temperature LSB	
24-25	All	Reserved	
26	All	Supply Voltage MSB	Internally measured module supply voltage
27	All	Supply Voltage LSB	
28-33	All	Reserved	

Channel Monitoring

Real time channel monitoring is for each transmit and receive channel and includes optical input power Tx bias current and Tx output Power. Measurements are calibrated over vendor specified operating temperature and

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voltage and should be interpreted as defined below. Alarm and warning threshold valuesshould be interpreted in the same manner as real time 16-bit data. Table 7 defines the Channel Monitoring.

Table 7 — Channel Monitoring Values

Byte	Bit	Name	Description
34	All	Rx1 Power MSB	Internally measured RX input power, channel 1
35	All	Rx1 Power LSB	
36	All	Rx2 Power MSB	Internally measured RX input power, channel 2
37	All	Rx2 Power LSB	
38	All	Rx3 Power MSB	Internally measured RX input power, channel 3
39	All	Rx3 Power LSB	
40	All	Rx4 Power MSB	Internally measured RX input power, channel 4
41	All	Rx4 Power LSB	
42	All	Tx1 Bias MSB	Internally measured TX bias, channel 1
43	All	Tx1 Bias LSB	
44	All	Tx2 Bias MSB	Internally measured TX bias, channel 2
45	All	Tx2 Bias LSB	
46	All	Tx3 Bias MSB	Internally measured TX bias, channel 3
47	All	Tx3 Bias LSB	
48	All	Tx4 Bias MSB	Internally measured TX bias, channel 4
49	All	Tx4 Bias LSB	
50	All	Tx1 Power MSB	Internally measured TX output power, channel 1
51	All	Tx1 Power LSB	
52	All	Tx2 Power MSB	Internally measured TX output power, channel 2
53	All	Tx2 Power LSB	
54	All	Tx3 Power MSB	Internally measured TX output power, channel 3
55	All	Tx3 Power LSB	
56	All	Tx4 Power MSB	Internally measured TX output power, channel 4
57	All	Tx4 Power LSB	
58-65			Reserved channel monitor set 4
66-73			Reserved channel monitor set 5
74-81			Reserved channel monitor set 6

Control Bytes

Control Bytes are defined in Table 8

Table 8 — Control Bytes

Byte	Bit	Name	Description
86	7-4	Reserved	
	3	Tx4_Disable	Read/write bit that allows software disable of transmitters.1
	2	Tx3_Disable	Read/write bit that allows software disable of transmitters.1
	1	Tx2_Disable	Read/write bit that allows software disable of transmitters.1
	0	Tx1_Disable	Read/write bit that allows software disable of transmitters.1
87	7	Rx4_Rate_Select	Software Rate Select, Rx channel 4 msb
	6	Rx4_Rate_Select	Software Rate Select, Rx channel 4 lsb
	5	Rx3_Rate_Select	Software Rate Select, Rx channel 3 msb
	4	Rx3_Rate_Select	Software Rate Select, Rx channel 3 lsb
	3	Rx2_Rate_Select	Software Rate Select, Rx channel 2 msb
	2	Rx2_Rate_Select	Software Rate Select, Rx channel 2 lsb
	1	Rx1_Rate_Select	Software Rate Select, Rx channel 1 msb
	0	Rx1_Rate_Select	Software Rate Select, Rx channel 1 lsb
88	7	Tx4_Rate_Select	Software Rate Select, Tx channel 4 msb (Not support)
	6	Tx4_Rate_Select	Software Rate Select, Tx channel 4 lsb (Not support)

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	5	Tx3_Rate_Select	Software Rate Select, Tx channel 3 msb (Not support)
	4	Tx3_Rate_Select	Software Rate Select, Tx channel 3 lsb (Not support)
	3	Tx2_Rate_Select	Software Rate Select, Tx channel 2 msb (Not support)
	2	Tx2_Rate_Select	Software Rate Select, Tx channel 2 lsb (Not support)
	1	Tx1_Rate_Select	Software Rate Select, Tx channel 1 msb (Not support)
	0	Tx1_Rate_Select	Software Rate Select, Tx channel 1 lsb (Not support)
89	All	Rx4_Application_Select	Software Application Select per SFF-8079, Rx Channel 4
90	All	Rx3_Application_Select	Software Application Select per SFF-8079, Rx Channel 3
91	All	Rx2_Application_Select	Software Application Select per SFF-8079, Rx Channel 2
92	All	Rx1_Application_Select	Software Application Select per SFF-8079, Rx Channel 1
93	2-7	Reserved	
	1	Power_set	Power set to low power mode. Default 0.
	0	Power_over-ride	Override of LPMode signal setting the power mode with software.
94	All	Tx4_Application_Select	Software Application Select per SFF-8079, Tx Channel 4 (Not
95	All	Tx3_Application_Select	Software Application Select per SFF-8079, Tx Channel 3 (Not
96	All	Tx2_Application_Select	Software Application Select per SFF-8079, Tx Channel 2 (Not
97	All	Tx1_Application_Select	Software Application Select per SFF-8079, Tx Channel 1 (Not
98-99	All	Reserved	
1. Writing "1" disables the laser of the channel.			

LPMode

The LPMode pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93 bits 0,1).

The module has two modes a low power mode and a high power mode. When the module is in a low power mode it has a maximum power consumption of 1.5W. This protects hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted. A truth table for the relevant configurations of the LPMode and the Power_over-ride and Power_set are shown in Table 9.

At Power up, the Power_over-ride and Power_set bits shall be set to 0.
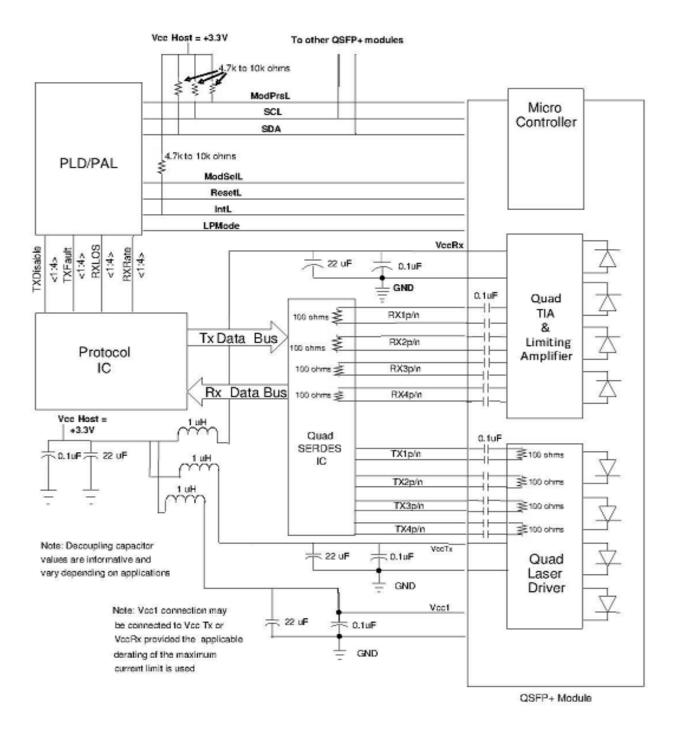
Table 9 —Power Mode Truth Table

LPMode	Power_Over-ride Bit	Power_set Bit	Module Power Allowed
1	0	X	Low Power
0	0	X	High Power
X	1	1	Low Power
X	1	0	High Power

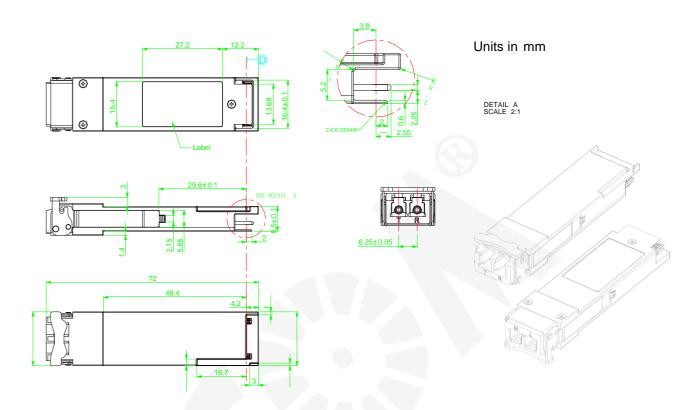SHENZHEN 6COM TECHNOLOGY CO., LTD   11/13
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7. Host - Transceiver Interface Block Diagram

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8. Outline Dimensions

Units in mm

DETAIL A
SCALE 2:1

9. Ordering information

Part Number	Product Description
6C-QSFP+-LR4	QSFP+,40Gb/s , 1271~1331nm,SMF, 10KM, DDM,LC connector, 0°C to 70°C

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