6C-CFP2-LR4

6COM,CFP2,100Gb/s ,1310,SMF,10KM,DDM, LC connector, 0°C to +70°C

FEATURES

- Direct LC receptacle optical interface
- Single +3.3V power supply
- Hot-pluggable
- Operating optical data rate up to 112Gbps
- Operating electrical serial data rate up to 27.952493Gbps
- 4 parallel electrical serial interface
- Transmission distance up to 10km
- AC coupling of CML signals
- 1310 nm window cooled EA-DFB LD
- PIN ROSA
- Low power dissipation (Max:12W)
- Built in digital diagnostic function
- Operating case temperature range:0℃ to 70℃
- Compliant with RoHs
- MDIO Communication Interface

APPLICATIONS

- OTN-OTU4
- Switch to switch interface
- Switch to rounter interface
- P to P Acess Network

STANDARDS

- Compliant with IEEE 802.3ba
- Compliant with CFP2 MSA hardware specification,Version1.0 July 31,2014
- Compliant with CFP MSA management specification，Version2.2July 01, 2013
- Compliant with ITU-T G.959.1
- Compliant with RoHS&WEEE

1. Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	°C	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	Vcc	V	-0.5	+3.6
Operating Case Temperature Range	Tc	°C	-5	75
Receiver Damage Threshold Per Lane	P_{dag}	dBm	+5.5	

2.Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tc	°C	0		70
Power Supply Voltage	Vcc	V	3.2	3.3	3.4
Data rate		Gb/s		103.125	112

3.Specifications (tested under recommended operating conditions, unless otherwise noted)

Parameter		Symbol	Unit	Min	Typ	Max	Notes
Voltage Supply Electrical Characteristics							
Supply Current	Tx Section	Icc	A	-	-	3.5	1
	Rx Section						
Power Supply Noise		Vrip				2%	DC-1MHz
						3%	1-10MHz
Dissipation	Class5	Pw	W			12	
Low Power Dissipation		Plow	W			2	
Inrush Current	Class5	I-inrush	mA/usec			200	
Turn-off Current		I-turnoff	mA/usec	-200			
Different Signal Electrical Characteristics							
Single Ended Data Input Swing			mV	55	-	525	
Single Ended Data Output Swing			mV	150	-	500	
Differential Signal Output Resistance			Ω	80		120	
Differential Signal Input Resistance			Ω	80		120	
3.3V LVCMOS Electrical Characteristics							
Input High Voltage		3.3VIH	V	2.0	-	Vcc+0.3	
Input Low Voltage		3.3VIL	V	-0.3	-	0.8	
Input Leakage Current		3.3IIN	uA	-10	-	+10	
Output High Voltage (I_{OH}=100uA)		3.3VOH	V	Vcc-0.2	-	-	
Output Low Voltage (I_{OL}=100uA)		3.3VOL	V			0.2	
Minimum Pulse Width of Control Pin Signal		t_CNTL	us	100			
1.2V LVCMOS Electrical Characteristics							
Input High Voltage		1.2VIH	V	0.84		1.5	
Input Low Voltage		1.2VIL	V	-0.3		0.36	
Input Leakage Current		1.2IIN	uA	-100		+100	
Output High Voltage		1.2VOH	V	1.0		1.5	
Output Low Voltage		1.2VOL	V	-0.3		0.2	
Output High Current		1.2IOH	mA			-4	
Output Low Current		1.2IOL	mA	+4			
Input Capacitance		Ci	pF			10	
Optical transmitter Characteristics							

Signaling Rate for Each Lan（100GbE）		Gbps	-	25.78125		
Signaling Rate for Each Lane（OTU4）				27.95249		
Four Lane Wavelength Range	λ1	nm	1294.53	1295.56	1296.59	
	λ2		1299.02	1300.05	1301.09	
	λ3		1303.54	1304.58	1305.63	
	λ4		1308.09	1309.14	1310.19	
Side Mode Suppression Ratio	SMSR	dB	30		-	
Total Average Launch Power	Pt	dBm	-		10.5	
Average Launch Power for Each Lane	Pa	dBm	-4.5		+4.5	2
Optical Modulation Amplitude for Each Lane	OMA	dBm	-1.3		4.5	3
Transmitter and Dispersion Penalty for Each Lanes		TDP			1.5	
Average Launch Power of Off Transmitter for Each Lanes	Poff	dBm	-		-30	
Extinction Ratio	ER	dB	7			
$RIN_{20}OMA$		dB/Hz			-130	
Optical Return Loss Tolerance		dB			20	
Transmitter Reflectance		dB			-12	4
Eye Diagram	Compliant with IEEE 802.3ba-LR4/OTU4					
Optical receiver Characteristics						
Receive Rate for Each Lane(100GbE)		Gbps	-	25.78125		
Receive Rate for Each Lane(OTU4)				27.95249		
Four Lane Wavelength Range	λ1	nm	1294.53	1295.56	1296.59	
	λ2		1299.02	1300.05	1301.09	
	λ3		1303.54	1304.58	1305.63	
	λ4		1308.09	1309.14	1310.19	
Overload Input Optical Power	Pmax	dBm	5.5			5
Average Receive Power for Each Lane(100GE)	Pa	dBm	-10.3		4.5	6&7
Average Receive Power for Each Lane(OTU4 with Tx ER of 4 to 6.5 dB)	Pa	dBm	-6.9		4.0	
Average Receive Power for Each Lane(OTU4 with Tx ER > 7 dB)			-8.8		2.9	
Receive Power In OMA for Each Lane	PinOMA	dBm	-		4.5	
Difference in Receive Power between Any Two Lanes		dBm	-		5.5	
Receiver Sensitivity in OMA for Each Lane(100GbE) at BER= $1x10^{-12}$	S_{OMA}	dBm			-8.6	8
Equivalent receiver sensitivity (OTU4 with Tx ER of 4 to 6.5 dB)	S_{AVG}	dBm			-8.4	9
Equivalent receiver sensitivity (OTU4 with Tx ER > 7 dB)					-10.3	9
Stressed Receiver Sensitivity in OMA for Each Lane(100GbE)		dBm			-6.8	10&11
Los Assert		dBm	-25		-13.6	
Los De-assert		dBm			-11.3	
Los Hysteresis		dBm	0.5			

Note1. The supply current includes CFP2 module's supply current and test board working current.

Note2. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance
Note3. Even if the TDP<1dB, the OMA (min) must exceed this value
Note4. Transmitter reflectance is defined looking into the transmitter
Note5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level
Note6. Minimum average receive power and maximum receiver sensitivity (OMA), each lane, is informative for 100GBase-LR4
Note7. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance
Note8. Receiver sensitivity (OMA), each lane (max) is informative
Note9. Measured with PRBS 2^{31}-1 for BER=10^{-5}. The BER for the OTU4 application is required to be met only after FEC has been applied.
Note10. Measured with conformance test signal at TP3 for BER=10^{-12}
Note11. Conditions of stressed receiver sensitivity test: vertical eye closure penalty for each lane is 1.8dB; stressed eye J2 jitter for each lane is 0.3UI; stressed eye J9 jitter for each lane is 0.47UI.

4. Hardware Control Pins

The CFP Module support real-time control functions via hardware pins, listed in the following table: Hardware Control Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
11	TX_DIS （PRG_CNTL）	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull-Up Note1
14	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up Note1
16	MOD_RSTn	Module Reset(Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down Note2

Note1: Pull-Up resistor (4.7KOhm to 10 KOhm) is located within the CFP module
Note2: Pull-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP module

5. Hardware Alarm Pins

The CFP Module supports alarm hardware pins listed in the following table: Hardware Alarm Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
15	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull-Down Note1
15	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull-Down Note1
12	RX_LOS （PRG_ALRM）	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

Note1: Pull-Down resistor (<100Ohm) is located within the CFP module. Pull-up should be located on the host

6. Management Interface Pins(MDIO)

The CFP Module supports alarm, control and monitor functions via an MDIO bus. The CFP MDIO pins are listed in the following table: Management Interface Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
13	GLB_ALRMn	Global Alarm	I	3.3V LVCMOS	Ok	Alarm	
18	MDIO	Management Data Input Output Bi-Directional Data	I/0	1.2V LVCMOS			
17	MDC	MDIO Clock	I	1.2V LVCMOS			
19	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	Per MDIO document [5]		
20	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
21	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			

7. Hardware Signaling Pin Timing Requirements

Timing Parameters for CFP hardware Signal Pins are listed in the following table.

Timing Parameters for CFP hardware Signal Pins

Parameter	Symbol	Min	Max	Unit	Notes&Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	Application Specific May depend on current state Condition when signal is applied .See Vendor Datasheet
Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert			ms	Value is dependent upon module start-up time.Please See register" Maximum High-Power-up ime"in "CFP MSA Management Interface Specification"
Receiver Loss of Signal Assert Time	t_loss_assert		100	us	Maximum value designed to support telecom applications
Receiver Loss of Signal De-Assert Time	t_loss_deassert		100	us	Maximum value designed to support telecom applications
Global Alarm Assert Delay Time	GLB_ALRMn_assert		150	ms	This is a logical "OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Global Alarm De-assert Delay Time	GLB_ALRMn_deassert		150	ms	This is a logical "OR" of Associated MDIO alarm&

					status registers.Please see MDIO document for further details
Management Interface Clock Period	t_prd	250		ns	MDC is 4MHz rate
Host MDIO t_setup	t_setup	10		ns	
Host MDIO t_hold	t_hold	10		ns	
CFP MDIO t_delay	t_delay	0	175	ns	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled(TX_DIS_asserted)	t_deassert		100	us	Application Specific
Transmitter Enabled(TX_DIS_asserted)	t_assert		20	ms	Value is dependent upon module start-up time.Please See register “Maximum TX-Turn-on Time” in “CFP MSA Management Interface Specification”

8. High Speed Electrical Characteristics

Reference Clock Characteristics（optional）

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency			161.1328125/644.53125		MHz	1/160 or 1/40 of electrical lane rate（100GE）
			174.7031 /698.8123MHz			1/160 or 1/40 of electrical lane rate（OTU4）
Frequency Stability	△f	-100		100	ppm	For Ethernet applications
		-20		20		For Telecom applications
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
RMS jitter[1,2]	σ			10	ps	Random Jitter Over frequency band of 10KHz<f<10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10%/90%	$t_{r/f}$	200		1250	ps	1/64 of electrical lane rate
		50		315		1/16 of electrical lane rate

Optional Transmitter and Receiver Monitor Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency					MHz	1/8 of Network lane rate
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	

9.Pin Description

The CFP2 connector has 104 pins which are arranged in Top and Bottom rows. The pin map is shown in table below. The detailed description of the Bottom row ranges from pin 1 through pin 52 and is shown Table below. The pin orientation is shown below in Figure below.

Figure : CFP2 Pin Map Orientation

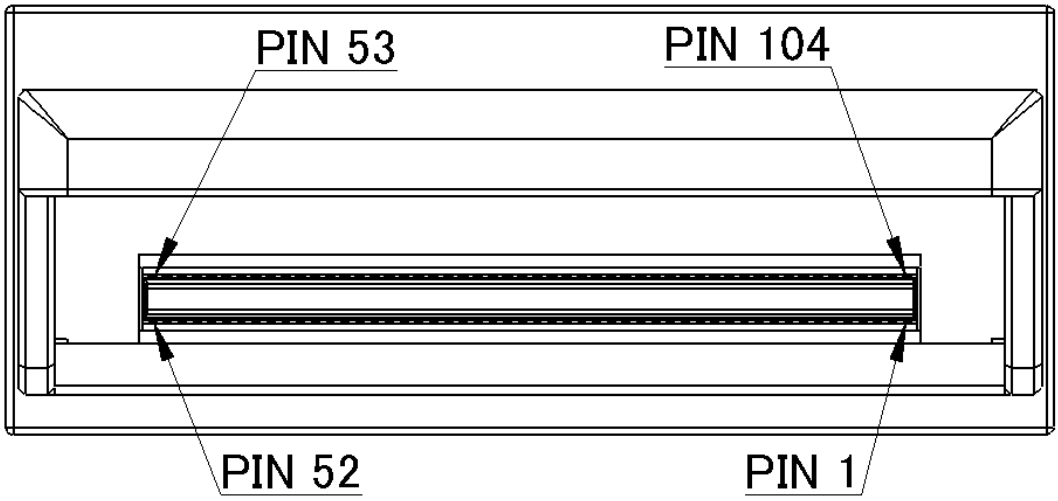


Table : CFP2 Pin-Map

1	GND	104	GND
2	(TX_MCLKn)	103	N.C.
3	(TX_MCLKp)	102	N.C.
4	GND	101	GND
5	N.C.	100	TX3n
6	N.C.	99	TX3p
7	3.3V_GND	98	GND
8	3.3V_GND	97	TX2n
9	3.3V	96	TX2p

10	3.3V
11	3.3V
12	3.3V
13	3.3V_GND
14	3.3V_GND
15	VND_IO_A
16	VND_IO_B
17	PRG_CNTL1
18	PRG_CNTL2
19	PRG_CNTL3
20	PRG_ALRM1
21	PRG_ALRM2
22	PRG_ALRM3
23	GND
24	TX_DIS
25	RX_LOS
26	MOD_LOPWR
27	MOD_ABS
28	MOD_RSTn
29	GLB_ALRMn
30	GND
31	MDC
32	MDIO
33	PRTADR0
34	PRTADR1
35	PRTADR2
36	VND_IO_C
37	VND_IO_D
38	VND_IO_E
39	3.3V_GND
40	3.3V_GND
41	3.3V
42	3.3V
43	3.3V
44	3.3V
45	3.3V_GND
46	3.3V_GND

95	GND
94	N.C.
93	N.C.
92	GND
91	N.C.
90	N.C.
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	N.C.
81	N.C.
80	GND
79	(REFCLKn)
78	(REFCLKp)
77	GND
76	N.C.
75	N.C.
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p
68	GND
67	N.C.
66	N.C.
65	GND
64	N.C.
63	N.C.
62	GND
61	RX1n
60	RX1p
59	GND

47	N.C.
48	N.C.
49	GND
50	(RX_MCLKn)
51	(RX_MCLKp)
52	GND

58	RX0n
57	RX0p
56	GND
55	N.C.
54	N.C.
53	GND

Table: Pin description

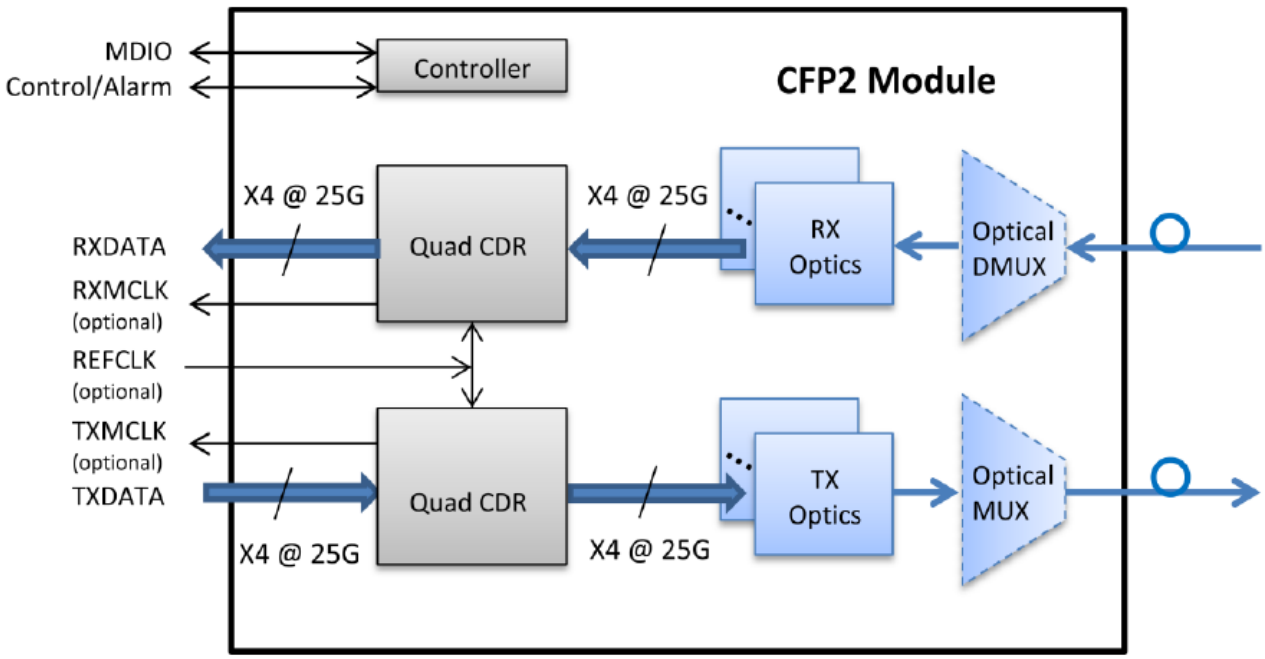
PIN#	Name	I/O	Logic	Description
1	GND			
2	(TX_MCLKn)	O	CML	For optical waveform testing. Not for normal use.
3	(TX_MCLKp)	O	CML	For optical waveform testing. Not for normal use.
4	GND			
5	N.C.			No Connect
6	N.C.			No Connect
7	3.3V_GND			3.3V Module Supply Voltage Return Ground,can be separate or tied together with Signal
8	3.3V_GND			
9	3.3V			3.3V Module Supply Votage
10	3.3V			
11	3.3V			
12	3.3V			
13	3.3V_GND			
14	3.3V_GND			
15	VND_IO_A	I/O		Module Vendor I/O A. Do Not Connect!
16	VND_IO_B	I/O		Module Vendor I/O B. Do Not Connect!
17	PRG_CNTL1	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
18	PRG_CNTL2	I	LVCMOS w/ PUR	Programmable Control 2 set over MDIO
19	PRG_CNTL3	I	LVCMOS w/ PUR	Programmable Control 3 set over MDIO
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO
23	GND			
24	TX_DIS	I	LVCMOS	Transmitter Disable for all lanes, “1” or

			w/PUR	NC=transmitter disabled,"0"=transmitter enabled
25	**RX_LOS**	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	**MOD_LOPWR**	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	**MOD_ABS**	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	**MOD_RSTn**	I	LVCMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	**GLB_ALRMn**	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	**GND**			
31	**MDC**	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
32	**MDIO**	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3-2012)
33	**PRTADR0**	I	1.2V CMOS	MDIO Physical Port address bit 0
34	**PRTADR1**	I	1.2V CMOS	MDIO Physical Port address bit 1
35	**PRTADR2**	I	1.2V CMOS	MDIO Physical Port address bit 2
36	**VND_IO_C**	I/O		Module Vendor I/O C. Do Not Connect!
37	**VND_IO_D**	I/O		Module Vendor I/O D. Do Not Connect!
38	**VND_IO_E**	I/O		Module Vendor I/O E. Do Not Connect!
39	**3.3V_GND**			
40	**3.3V_GND**			
41	**3.3V**			3.3V Module Supply Voltage
42	**3.3V**			
43	**3.3V**			
44	**3.3V**			
45	**3.3V_GND**			
46	**3.3V_GND**			
47	**N.C.**			No Connect
48	**N.C.**			
49	**GND**			
50	**(RX_MCLKn)**	O	CML	For optical waveform testing. Not for normal use.
51	**(RX_MCLKp)**	O	CML	For optical waveform testing. Not for normal use.
52	**GND**			
53	**GND**			
54	**N.C.**			
55	**N.C.**			

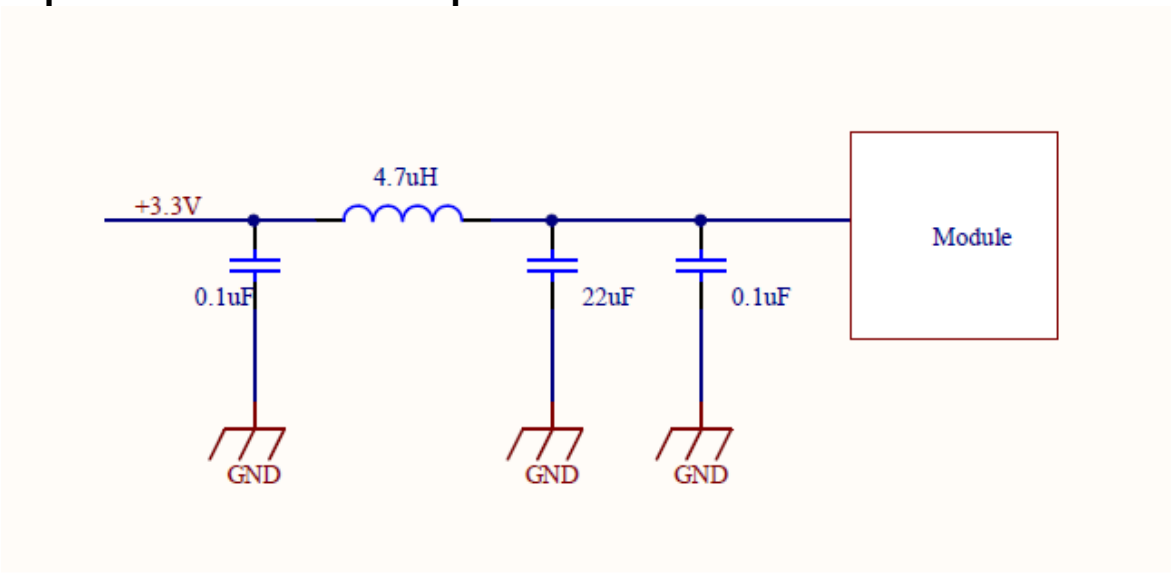
56	**GND**			
57	**RX0p**	O	CML	Output Data
58	**RX0n**	O	CML	Inverted Output Data
59	**GND**			
60	**RX1p**	O	CML	Output Data
61	**RX1n**	O	CML	Inverted Output Data
62	**GND**			
63	**N.C.**			
64	**N.C.**			
65	**GND**			
66	**N.C.**			
67	**N.C.**			
68	**GND**			
69	**RX2p**	O	CML	Output Data
70	**RX2n**	O	CML	Inverted Output Data
71	**GND**			
72	**RX3p**	O	CML	Output Data
73	**RX3n**	O	CML	Inverted Output Data
74	**GND**			
75	**N.C.**			
76	**N.C.**			
77	**GND**			
78	**(REFCLKp)**			
79	**(REFCLKn)**			
80	**GND**			
81	**N.C.**			
82	**N.C.**			
83	**GND**			
84	**TX0p**	I	CML	Input Data
85	**TX0n**	I	CML	Inverted Input Data
86	**GND**			
87	**TX1p**	I	CML	Input Data
88	**TX1n**	I	CML	Inverted Input Data
89	**GND**			

90	**N.C.**			
91	**N.C.**			
92	**GND**			
93	**N.C.**			
94	**N.C.**			
95	**GND**			
96	**TX2p**	I	CML	Input Data
97	**TX2n**	I	CML	Inverted Input Data
98	**GND**			
99	**TX3p**	I	CML	Input Data
100	**TX3n**	I	CML	Inverted Input Data
101	**GND**			
102	**N.C.**			
103	**N.C.**			
104	**GND**			

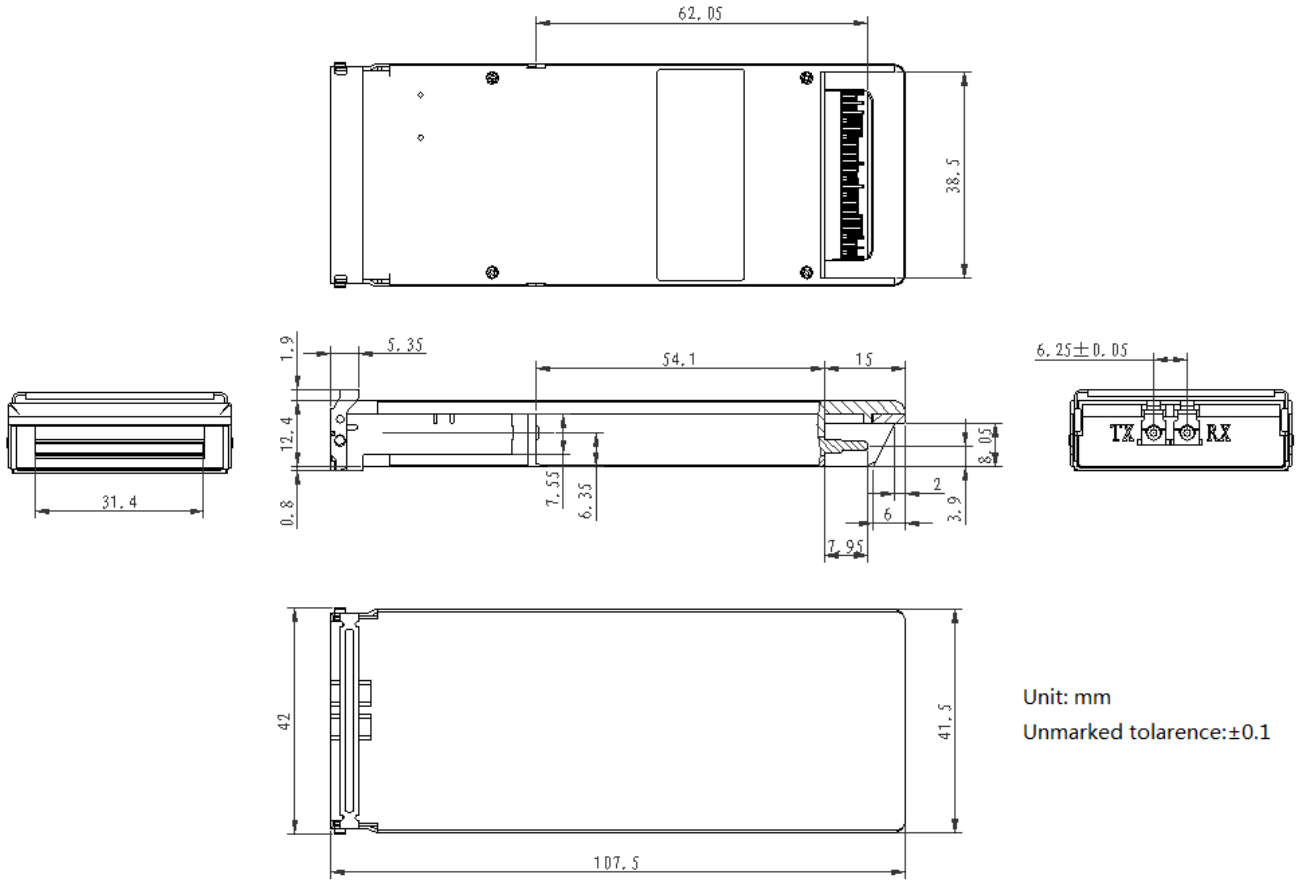
Block diagram



10. Required Host Board Components



11. Package outline



12. Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	high speed signal pins shall withstand 500V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B the other pins with exception of the high speed signal pins shall withstand 2kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B
Electrostatic Discharge (ESD) Immunity	IEC61000-4-2 Class B	15kV air discharges during operation and 8kV direct contact discharge
Electromagnetic Interference (EMI)	CISPR22 ITE Class B FCC Class B CENELEC EN55022 VCCI Class 1	Compliant with standard
Immunity	IEC61000-4-3 Class 2	Compliant with any electo-magnetic regulations
Safety	FDA CDRH 21-CFR 1040 Class 1	
	UL	
	TUV-GS	
	CE	

13. Ordering Information

Part No	Specifications									Application Code
	Pack	Data rate	Tx	Pout	Rx	S	Top	Reach	Others	
6C-CFP2-LR4	CFP2	103.125 Gbps ~112 Gbps	1310nm LAN Cooled EMA DFB-LD	-4.3~ +4.5 dBm	PIN	<-10.3 dBm	0~ 70° C	10km	DDM	100GbE/OTU4